SYNOPSYS®


# Welcome to the HSPICE Newsletter—2005 Spring Edition.

**Contents:**



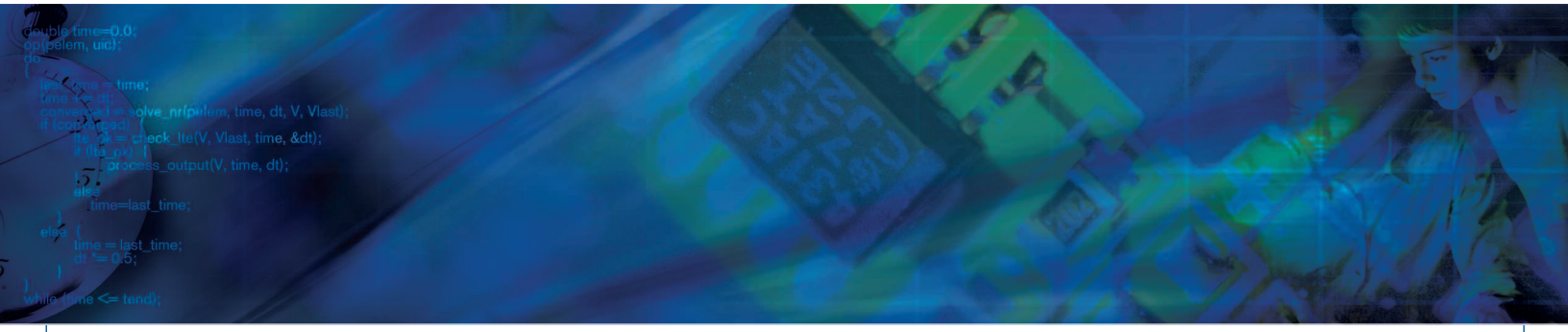
It gives me great pleasure to greet our loyal HSPICE® users and thank you for your continued support.

In the past 2 years, HSPICE has significantly enhanced several key features and capabilities while continuing to maintain the highest simulation accuracy. Some of these features, introduced in past releases, include considerable improvement in simulation performance, better convergence, STI/LOD stress model, differential and mixed S-parameter support and improved accuracy in W-element. Last September, for the 2004.09 release, we introduced HSPICE RF, an add-on option to HSPICE, which provides high-performance, high-capacity steady-state RF simulation capability with the same usage and models as HSPICE.

This HSPICE Newsletter contains an overview of new features in HSPICE 2005.03 release and a section on frequently asked questions. Among the many new features are behavioral and device models with Verilog-A, proprietary HVMOS and TFT device models developed by Synopsys, and enhanced RF capabilities. These features are detailed in the documentation, and to make it easier, we have included an article about how to efficiently search the documentation.

Circuit simulation has increased in complexity and the needs of the circuit designer have become more demanding. We will to continue to address these complex needs in the most effective manner and continue to meet your expectations of HSPICE—the gold standard in accurate circuit simulation.

Don MacMillen,
V.P. Engineering
AMS & Custom Design



# HSPICE with Verilog-A: Salient Features

In today's highly competitive analog and mixed signal IC market, minimizing product-to-market time is essential to ensure success of the products and even the company. Verilog-A has been shown to be an ideal language for describing analog behavior, including implementation of compact device models. It efficiently describes and verifies analog and mixed signal IC and large system-on-a-chip (SoC) designs which contain analog circuits, digital-logic blocks, memories, and processing capability on the same piece of silicon. Verilog-A supports both a top-down design as well as a bottom-up verification methodology.

The HSPICE Verilog-A implementation allows Verilog-A model simulation in HSPICE—it supports a mixed design of Verilog-A descriptions and transistor-level SPICE netlists with great ease of use. The compiler-based solution results in simulation times comparable to built-in models. All major analysis features available in HSPICE are supported on Verilog-A based devices.

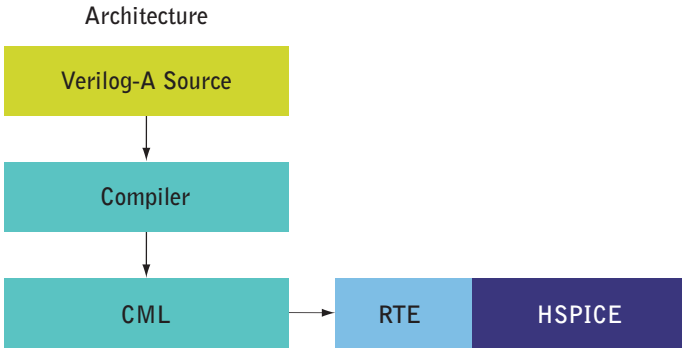
> "The HSPICE Verilog-A implementation allows Verilog-A model simulation in HSPICE–it"

## Specifications:

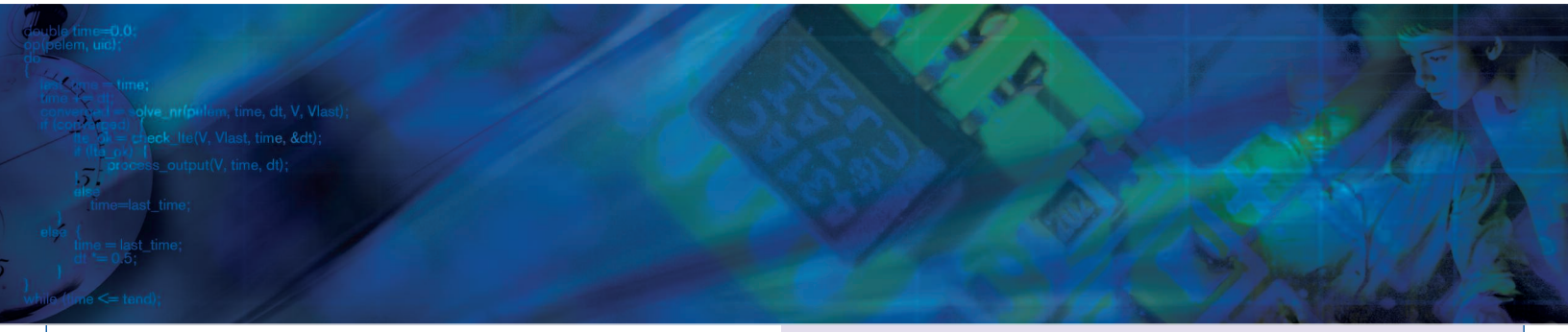
1. Supported HSPICE Verilog-A language features:
   - Supports Verilog-A language features defined in "Analog language subset" of Verilog-AMS Language Reference Manual 2.1.
2. Supported HSPICE Verilog-A features:
   - Supported by existing HSPICE netlist syntax. You are not required to learn new syntax to use Verilog-A based devices in HSPICE netlists.
   - Supports all major HSPICE analysis types, including AC, DC, transient, Statistical Analysis, and Optimization.
3. Seamless design and verification flow with a compiled Verilog-A Solution:
   - Verilog-A models are instantiated like HSPICE subcircuits—they use the same element as the subcircuit element, the 'X' element. Verilog-A models contained within circuit netlists are automatically compiled or recompiled on-the-fly only when necessary.

## Solution:

Verilog-A models are instantiated like HSPICE subcircuits—they use the same element as the subcircuit element, the 'X' element. Verilog-A models contained within circuit netlists are automatically compiled or recompiled on-the-fly only when necessary.




CML= Compiler Model Library
RTE= Run Time Environment



**Usage Model Overview**

```
*Simple Verilog-A amplifier
.hdl amp.va
vs 1 0 1
rs 1 0 1
xl 1 2 my_amp gain=10
rl 2 0 1
```

```
module va_amp(in, out);
parameter real gain = 1.0;
electrical in, out;
analog begin
    V(out) <+ gain * V(in);
    end
endmodule
```

1. Verilog-A modules are loaded into the system via a new command the ".hdl" netlist command or the –hdl HSPICE command-line option.
2. Modules are instantiated in the same manner as HSPICE subcircuits.
3. Verilog-A device data can be output using conventional output commands.

As circuit complexities continue to grow and time to market pressures intensify, new approaches leading to more robust circuit simulation will be adopted. We believe that the use of Verilog-A in HSPICE (available in the 2005.03 Release) will be a great utility to circuit designers

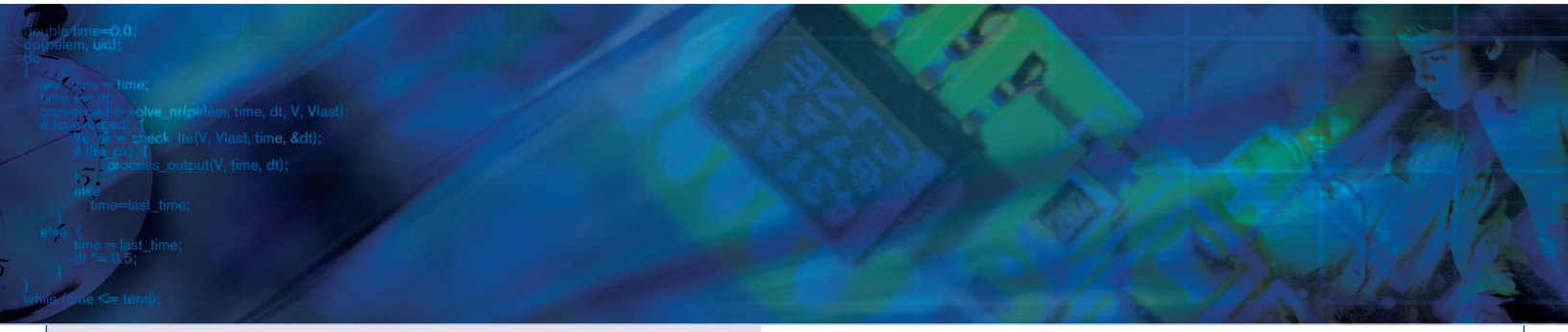
## HSPICE with Verilog-A: Customer Viewpoint

**Dr. Geoffrey Coram, Analog Devices, Inc.**

Analog Devices, Inc. is a leading manufacturer of high-performance analog circuits. Our circuit designers frequently need better transistor models than the standard models implemented in commercial simulators, or need new features before those features are added to the standard models. For example, our internal high-speed bipolar processes have significant self-heating, but this effect is not captured in the standard Gummel-Poon model. Our designers needed to model this effect well before the arrival of the new bipolar transistor models such as Mextram 504 and HICUM. On the CMOS side, our designers needed models that accounted for the pocket implant effect before CMOS foundries were producing BSIM4 model libraries.

Verilog-A gives us the ability to modify the existing standard models – or even to create our own models from scratch – and perform circuit simulations with them. The language itself was designed for analog modeling, which makes it much more convenient to use than a C-based "common model interface" (CMI). Furthermore, unlike a CMI, Verilog-A is simulator-independent, so a model written in Verilog-A will run in a traditional Spice simulator like HSPICE as well as a fast-Spice simulator like NanoSim or an RF simulator (HSPICE-RF support for Verilog-A is expected later this year)—as well as in some parameter extraction software.

I had the opportunity to evaluate a pre-release version of HSPICE with Verilog-A. The netlist syntax was straightforward to use, as can be seen in the usage model overview in the previous article. Model cards are supported for Verilog-A modules, which is a critical factor when writing transistor models in Verilog-A: such models typically have tens to hundreds of parameters which can be collected into a model card rather than specified repeatedly for each instance.



Support for all the features I needed from Verilog-AMS LRM version 2.1 was present, though I am eager to see inclusion of device modeling extensions to the language in version 2.2.

> "…..in small analog circuits, speed is not often an issue, getting the right answer is."

I simulated some test circuits using a Verilog-A definition of BSIM3. As promised, I was able to run transient, dc, ac, and noise analyses, and the results generally matched those from running with the build-in BSIM3 (mos level 49). The Verilog-A simulations in the pre-release code were slower, by a factor of less than 2 in transient analysis and about a factor of 3 in a dc sweep. Small-signal ac and noise analyses experienced essentially no degradation in speed, which one should expect from the algorithms they use. While the speed degradation is undesirable (and Synopsys is undoubtedly working to improve this for the full release), in small analog circuits, the speed is not often an issue, getting the right answer is. The ability to include custom device models is a welcome addition to HSPICE.

## Lossy Transmission Line Simulation Using S-Parameter

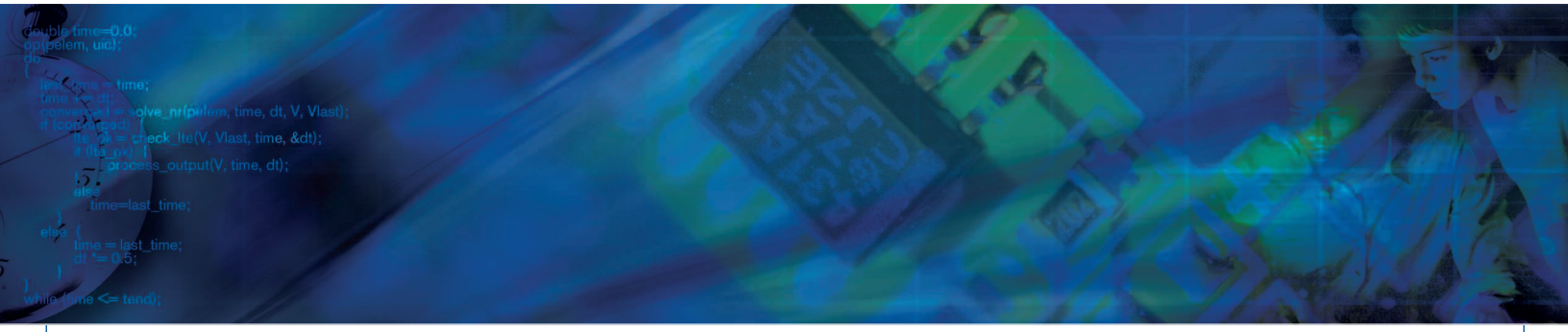
In HSPICE, S (scattering) parameters can be used to describe many kinds of multi-port systems. Certain packages, traces, connectors, backplanes, and cable sections, measured data or 3-D EM solver data for transmission line systems are often available in the form of S-parameters. Now W-element in HSPICE has added a new degree of usability. It can accept measured data from a network analyzer, namely Scattering parameter as input for circuit simulation and analysis. Previously, the users were limited to the geometry supported by a 2-D field solver or third party 3-D field solver program.

The advantage of the S-parameter input for transmission line:

- Measured data is used directly in simulation
- Efficiently validate field solver models
- Exact representation of frequency dependent behavior
- Compliment with the 2-D field solver in HSPICE

HSPICE originally has two elements that support frequency dependent characteristics of multi-port networks. One is the S-element that accepts arbitrary types of multi-port networks described in S-parameters. The other is the W-element that accepts ideal or lossy transmission line based frequency dependent RLGC parameters.

> "W-Element in HSPICE ..can accept measured data from a network analyzer, namely Scattering parameter as input for circuit simulation and analysis"



Since our experiences have showed us that many of HSPICE S-element users are attempting to model transmission line systems with S-parameters, in the case that users can explicitly tell HSPICE that the input S-parameters are based on transmission line system, it is ideal for HSPICE to handle these parameters as transmission lines input. . The added advantage is that S-parameters can now be scaled through W-element.

Based on these considerations above, we have introduced a new function of the W-element in the 2005.03 release to accept transmission line based S-parameters by allowing the user to specify W-element instances associate with S-parameter models.

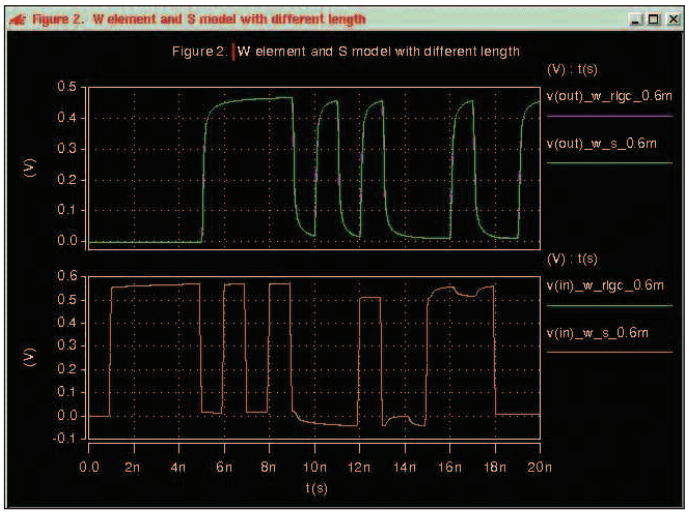
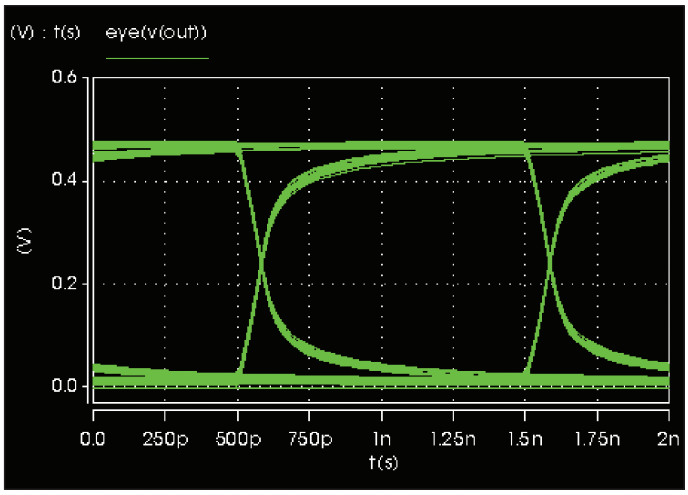
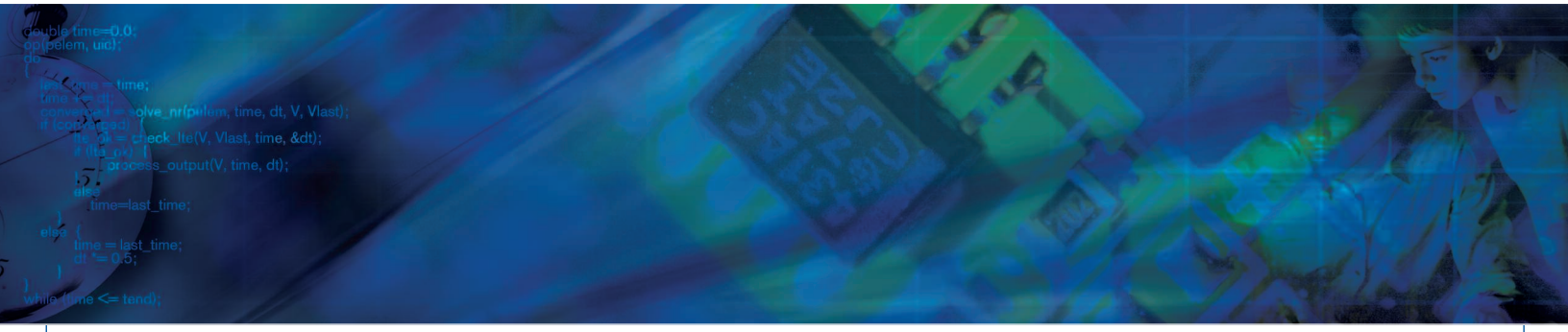



Fig showing W- Element and S-model with different line length




Example circuit shown eye diagram of a W element with 400 ns transient with 2X line length to show relative significant loss



## New Synopsys-developed Device Models

HSPICE has supported 'Foundry-Certified' device models and continues to be the technology leader in commercially available device models. For the March 2005 release, HSPICE introduces 2 new Synopsys-developed device models.

### TFT Device Model

This is a Poly silicon TFT (thin film transistor) device that serves as the mainstream drivers for TFT LCD display technology. HSPICE has incorporated three major enhancements into its Level=62 poly silicon TFT device model:

1. Enhancements to include the "version 2" of the RPI poly silicon TFT model. These include improvements in the field dependence of channel carrier mobilities, the output resistance model, the modeling of floating body effects, and the overall continuity of the model formulations.
2. Addition of self heating thermal model.
3. HSPICE ACM model.

### HVMOS Device Model

HSPICE has recently developed an accurate and versatile HVMOSFET device model (Level=66) for various HVMOS device processes and structures, to meet the ever increasing need for the high voltage CMOS technology in applications such as LCD displays, telecommunications, and automotive, computer and consumer electronics products. This model takes into account all the unique and critical physical effects found in high voltage CMOS operations. Unparalleled modeling accuracy and parameter extraction easiness have been accomplished through intensive beta testing.

## FAQ's

**Customer Question #1:** I have a VCO netlist. I am doing a transient analysis, sweeping the control voltage to get a tuning curve (frequency versus control voltage). The VCO is supposed to oscillate for the entire range of control voltages. But for some control voltage values the VCO simulation does not show oscillation. Are there any recommended options for simulating this VCO?

**Answer:** Most likely, the netlist is missing a .ic or other stimulus to kick start the oscillation. The easiest remedy is to add a .ic command such as:

```
.ic v(node1)=0
```

Without the .ic, the oscillator starts at time=0 in an unstable symmetric steady state condition. With this starting point, the simulation relies on numerical round off and tolerances to start the oscillator.

When you add the .ic, the time=0 state is forced to an asymmetric state which guarantees oscillator startup.

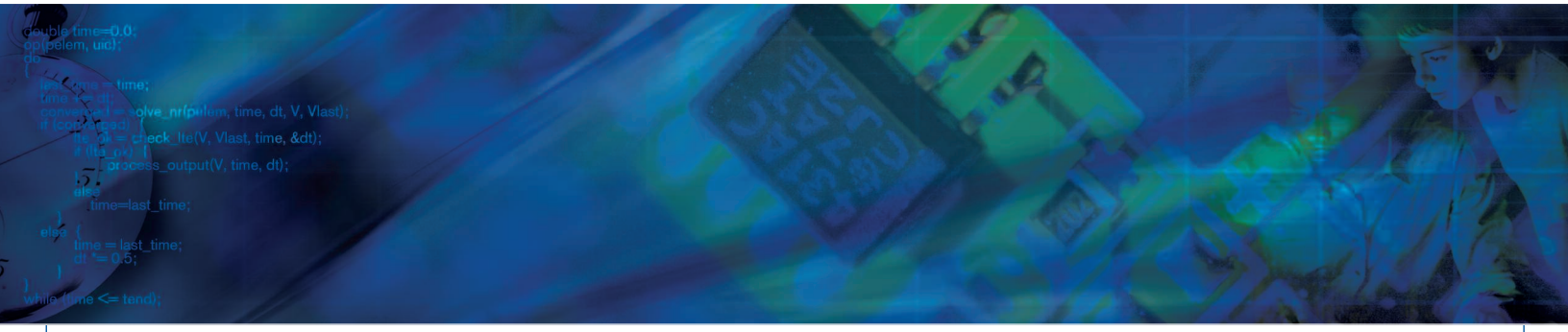
The next question is: Which node do you select for the .ic? For a ring oscillator, choose one of the nodes in the ring. For an LC oscillator, the inductor current is often a good choice, as in:

```
L1 n1 n2 200n ic=1u
```

Instead of .ic, another way to start the oscillator is to use a time varying stimulus. For example, you could ramp the power supply up from zero, or inject a current pulse, as in:

```
Vdd vdd 0 pwl(0 0 1n 3)  or  istart 0 n1 pwl
(0 0 0.1n 1u 0.2n 1u 0.3n 0)
```

An alternate way to generate this VCO frequency vs. bias curve is to use HSPICE RF's oscillator steady-state analysis. HSPICE RF



works faster because it directly computes the steady state solution and so avoids the long transient startup.

This can speed up the simulation time quite a bit. In one particular case, we found that the transient simulation in HSPICE took about 160 seconds per control voltage point, so for 171 bias points it took over 7.5 hours. We were able to run this simulation with HSPICE RF in about 18 minutes, obtaining the same frequency vs. control voltage curve.

The latest HSPICE RF version is 2005.03 and is currently available.

**Customer Question #2:** When solving for a DC convergence error, I noticed that the diagnostic message did not contain any problem element or node? Is this always the case? Can I get a diagnostic report with more details?

**Answer:** HSPICE auto-converge process, which is on by default, suppressed the printing of the non-convergence diagnostic table. However setting the following options,

```
.OPTION CONVERGE=-1 DCON=-1,
```

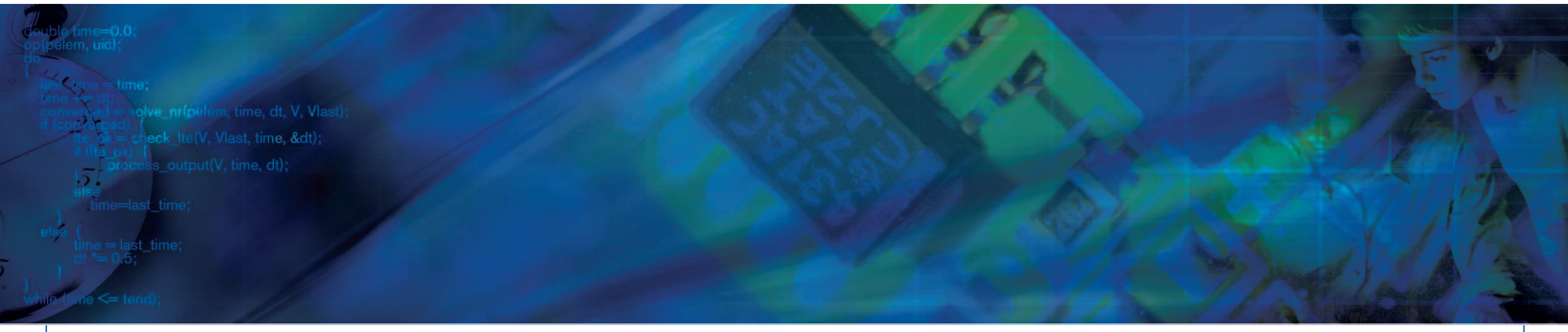
will generate two diagnostic tables for debug:

- Print out of all non-convergent nodal voltages, and the associated voltage error tolerances.
- Print out of all non-convergent elements, and their associated element currents, element voltages, model parameters, and current error tolerances.

**Customer Question #3:** Could you please explain how to use HSPICE bisection analysis to find the optimal setup time for a latch?

**Answer:** Characterization of latches for setup/hold can be very difficult. The user must diligently use the HSPICE bisection optimization to achieve the results. One of the settings to calculate setup time is given below.

```
V2 EN 0 PWL(0 1.200000
+ 30000.000P 1.200 '40001.000P-ref_value' 1.200
+ '40011.000P-ref_value' 0.000)

V1 DATA 0 PWL(0 0.000000
+10000P 0.000000 10010P 1.200000
+20000P 1.200000 20010P 0.000000
+30000.000P 0.000 '30001.000P+ref_value' 0.000
+'30011.000P+ref_value' 1.200)

.PARAM ref_value = Opt1 (0.000P, 0.000P, 10000.000P)

.MEASURE Tran setup
+    TRIG V(EN) VAL=0.600 FALL=1 td=30000.000P
+    TARG V(DATA) VAL=0.600 RISE=1 td=30000.000P

.MEASURE Tran vmax0
+ MAX par('V(Q)-0.600') from=30000.000P

.MEASURE Tran vmax1
+ MAX par('0.600-V(QN)') from=30000.000P

.MEASURE Tran OutResult
+ PARAM = "max(vmax0, vmax1)" GOAL = 0
.MODEL OptMod Opt Method = Bisection

.TRAN 10000P 30000.000000P 10ps 50021P
+    Sweep
+    Optimize = Opt1
+    Result = OutResult
+    Model= OptMod
```



In the above strategy, the failure criterion is set as the enable pin (EN) going inactive. The bisection analysis might fail if the settings are not correct. The optimization parameter limits must be chosen in such a way that they satisfy pass/fail condition of the result criterion. It is also necessary to check whether the input/output changes are taking place as expected.

Library characterization tools (most of them use HSPICE) employ a number of techniques for characterization. Synopsys library characterization tool, STAR-MTB, is very effective in characterizing latches and other sequential cells using HSPICE bisection optimization.

**Customer Question #4:** I have always used .Option ACCURATE in my circuit simulations. Is this always needed? When is this option not helpful?

**Answer:** Using .OPTION ACCURATE is not always needed. It largely depends on what are you going to do with the simulation results. Take library characterization for example, if the simulation results are used for building and characterizing behavioral models for digital designers, then the default HSPICE setting should be accurate enough. If the simulation results are used for custom IC and analog circuit design, then the accurate setting is needed.

However in this case, we would recommend use of RUNLVL option when possible. Setting option RUNLVL=5 uses tolerances which are similar to option ACCURATE. You can use .opt ACCURATE in conjunction with RUNLVL, in which case HSPICE will also set bypass=0 and enforce a minimum RUNLVL setting of 5. RUNLVL not only maintains the desired accuracy, but also improves the simulation speed for a large number of cases.

**Customer Question #5:** I find that HSPICE sometimes takes a long time to invoke a license. Are there any recommendations to improve license check out time for HSPICE?

**Answer:** Some applications have experienced a slower initialization when the license environment variable points to a large license file list or a long list utilizing the license file path instead of the port@host notation. Since the Synopsys License Manager Daemon (snpslmd) server has pooling implemented, applications could take longer to initialize if the license file list is very long.

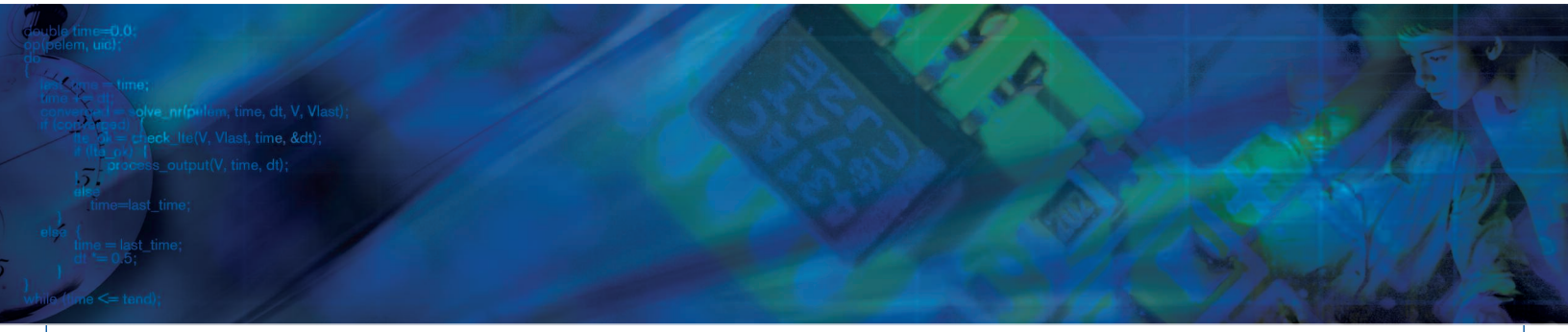
Some of the guidelines to work-around the performance issue are:

- Use minimum number of license servers in the licensing environment variable.
- Always try to use the port@host notation.
- If the licensing variable list is long, put the local license server at the beginning of the list.
- If the licensing variable list is long, then eliminate all the license servers that are over a WAN(Wide Area Network).
- If unable to use the above work-around, set SCL_POOL_OPTION=OFF. This will disable pooling for the application, thereby preventing this issue.

**Customer Question #6:** I am using encrypted models and I am getting warnings and errors, but I cannot figure out what is wrong. Is there any way to know why these are occurring?

**Answer:** If the warning or error is caused by an encrypted block, HSPICE will not reveal any node or element information from the encrypted block the warning or error comes from. You will get either:

```
"**warning** associated with encryp ted blocks were
suppressed due to encrypted content"

or

"**error** in encrypted blocks, please contact
encrypted file provider"
```



You will need to contact the provider of the encrypted blocks that you are using to help troubleshoot your circuit.

## HSPICE Documentation: Finding What You Need

When you are looking for a specific topic in the HSPICE documentation, users typically:

1. Use the table of contents or
2. The index to find information within each individual HSPICE manual.

But did you know that there is also a way to search all of the HSPICE documentation for a particular topic or keyword all at once? With the help of Adobe Acrobat's full-text search function, you can!

Included on the HSPICE CD, in your HSPICE EST download, or on the SOLD (Synopsys Online Documentation) CD, is a file named "index.pdx" that contains an index of all of the HSPICE manuals for the 2005.03 release. This is an index of all the content that exists in the HSPICE 2005.03 documentation set. To use this index, use the instructions that follow.

**NOTE:** Due to an Acrobat limitation, full-text search indexes are not supported on the Linux platform.

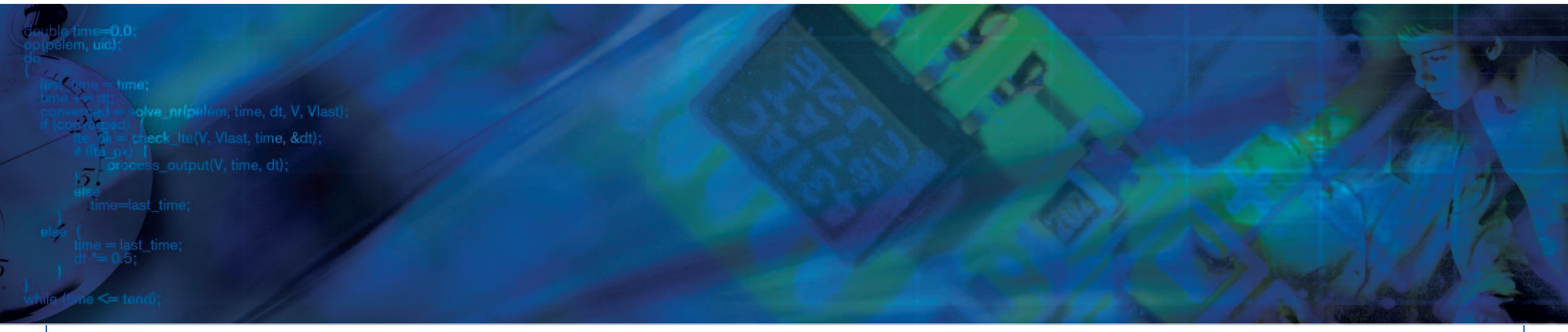
If you have Acrobat Reader 6.0, you do not need to load the "index.pdx." Follow these instructions to search several PDFs at the same time:

1. Make sure all of the PDFs you wish to search are in one directory.
2. Open Acrobat Reader 6.
3. Choose Edit > Search to open the search pane.
4. In the "Where would you like to search?" section, click the radio button next to the "All PDF documents in."
5. Click the drop down menu and choose "Browse for Location… ." The "Browse for Folder" window appears.
6. In the directory hierarchy, locate and select the directory that contains the PDFs you want to search and click OK.
7. Enter a search term in the search pane and click the "Search" button. Acrobat searches all of the documents in the selected directory and gives you a list of the occurrences within each manual. Clicking a link brings you to the exact location of each occurrence of your search term.

### For Acrobat Reader 4.0 and 5.0

To search several PDFs at the same time, you need to load the "index.pdx" file into Acrobat. To load the "index.pdx" file, follow these instructions:

1. Ensure you have all of the HSPICE PDFs, Index directory, and "index.pdx" file all in one directory.
2. Open Acrobat Reader 4.0 or 5.0.
3. Choose Edit > Search > Select Indexes… from the menu bar. The "Index Selection" window appears.
4. In the "Index Selection" window, click the "Add…" button. The "Add Index" window opens.
5. Browse to the location where you have all of your PDFs and index.pdx file saved.
6. Once located, select the "index.pdx" file and click OK.
7. In the "Index Selection" window, make sure the check box to the left of the last index title is checked. No other indexes should be selected.
8. Click OK. The full-text search index for the HSPICE manual set is now loaded.

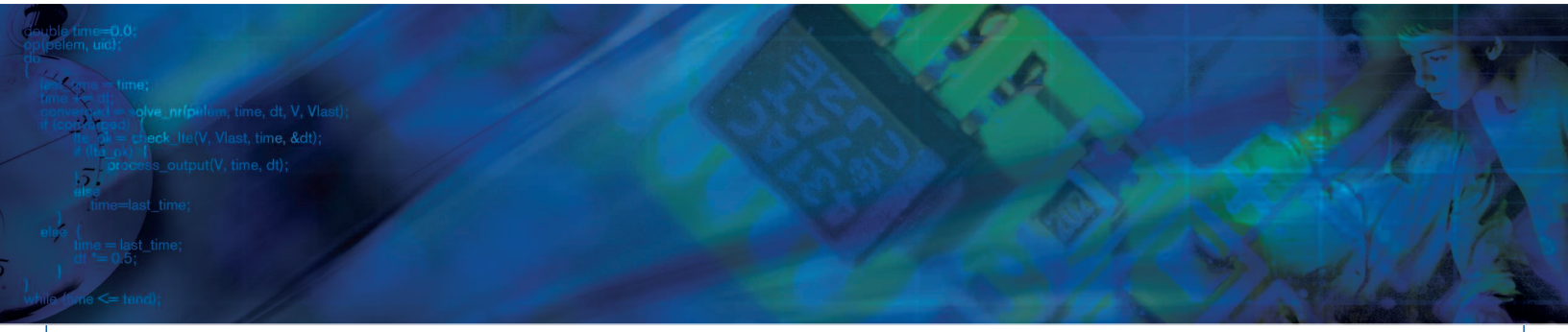


### To search the HSPICE PDFs using the full-text search index:

1. Choose Edit > Search > Query… from the menu bar. The “Adobe Acrobat Search” window appears. A message appears at the bottom of the window stating which index is loaded. Make sure it reads “Searching in the Synopsys HSPICE, W-2005.03 index.” If this does not appear, you need to load the full-text search index. See the previous instructions on how to do this.
2. Enter a search term and click the “Search” button. A list of manuals that contain your search term appears.
3. Double-click on the title of the manual you wish to further your search. The selected manual opens to the first page that Acrobat finds your search term.
4. You can find other occurrences of your search term by choosing Edit > Search > Next from the menu bar.

More help is available in Acrobat Reader 4.0 or 5.0 help under the “Searching Catalog Indexes” section.

### Email feedback/comments to: HSPICEnews@synopsys.com



## Resources

Synopsys website: www.synopsys.com

Synopsys University Program website: http://www.synopsys.com/partners/university

Online documentation and access to web-based problem-resolution support service: SolvNET®

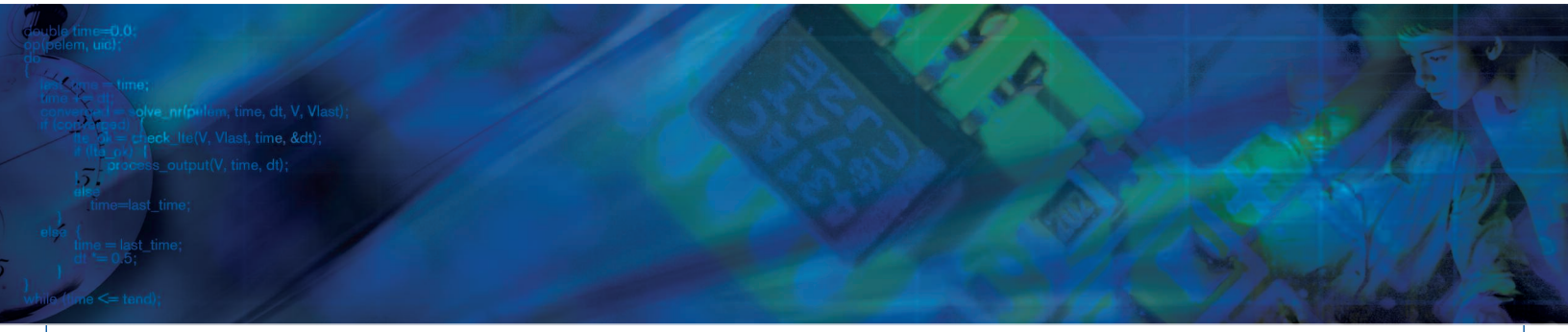
Synopsys tool-training workshops are available to professors at any Synopsys training center: Synopsys Customer Education.

SVP Café℠ - online information center for the latest semiconductors vendors news, products and support for Synopsys:
http://www.synopsys.com/svpcafe/

EE Times, electronics industry publication www.eetimes.com

Design Automation Conference www.dac.com

www.HSPICE.com



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