AN1591
APPLICATION NOTE

STLC60133 SMALL SIGNAL SPICE MODEL

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This document outlines the small signal SPICE model of the STLC60133 xDSL Line Driver, a dual amplifier featuring a large bandwidth optimized for XDSL applications.

Information about model features and limits, indication on model utilization and test circuit schematics are included.

INTRODUCTION

STLC60133 small signal SPICE model is a simulation model of the STLC60133 xDSL Line Driver for AC analysis.

It is a simplified but accurate derivation of the complete Eldo® description of the circuit.

xDSL systems performances heavily depend on Line Drivers features as distortion, noise and bandwidth. Distortion and noise are parameters very difficult to simulate with a simplified model, even using a full transistor model results are very far from the precision needed by an xDSL system.

The value of a model lies on its capability to simulate reality, and the need of a simplified model comes from computing resources, these are the reasons why we focused our model only on small signal features.

Those allow evaluating device compatibility with different application circuits (Line Interfaces) and main features of its AC behavior.

Overall circuit performances should be verified with laboratory testing.

Following sections describe model features, limits and performances.

FEATURES

STLC60133 small signal SPICE model is the small signal model of the STLC60133 xDSL line driver.

It models one of the two amplifiers that compose the STLC60133.

The model of the complete device is simply the union of two of these models, forming 4 inputs (IN1P, IN1N, IN2P, IN2N), 2 outputs (OUT1, OUT2) device.

Active devices are modeled through their small signal models (hybrid π model for transistors and small signal conductance for diodes), all components relevant parasitic resistance and capacitance has been taken into account.

This model has been designed to run an AC analysis to evaluate STLC60133 performances when it is connected inside an application circuit, usually a line interface scheme.

Testable characteristics are:

- Frequency response
- Input impedance
- Output impedance
- Open loop differential gain
- Stability

These parameters are well modeled till frequencies above a few hundred MHz, than the effect of parasitic component begin more relevant and a direct laboratory testing is advised.

LIMITS

To use the STLC60133 small signal SPICE model in a correct way, model limits have to be clearly kept in mind.

They are mainly the ones of a small signal model, this means that characteristics such as distortion, slew rate, output dynamic, output current capability and variation with temperature can not be simulated.

Neither can be run DC nor transient analysis.

TEST CIRCUIT SCHEMATIC

Circuit schematic used to test model performances versus complete STLC60133 Eldo® model, is described in this section.

It helps to understand and verify model features.

Special interest feature of the model is the frequency response of the Line Driver in an Open Loop configuration.

As specified in [1] SPICE techniques permit the use of particular methods to obtain accurate gain and phase information for closed-loop analog circuits that use negative feedback.

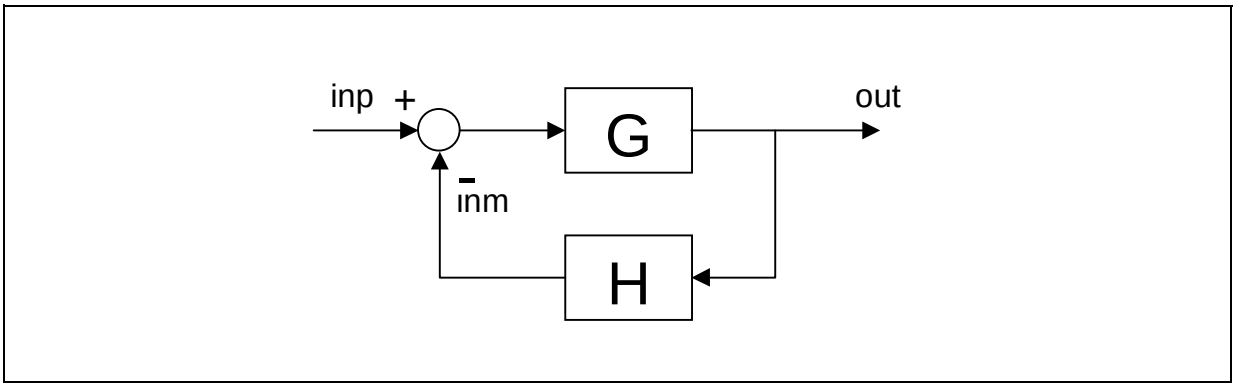
More precisely, Open Loop Gain (OLG) can be evaluated by collecting the potential of the input nodes in a non-inverting closed loop configuration.

The OLG is then given by the ratio:

$$V(inm)/(V(inp)-V(inm)) \quad (1)$$

Looking at a tipycal loopback scheme:

Figure 1. Loopback scheme



It can be seen that

$$inm = H * out \quad (2)$$

So

$$H = inm / out \quad (3)$$

at the same time

$$out = G * (inp - inm) \quad (4)$$

so

$$G = out / (inp - inm) \quad (5)$$

the OLG is defined as the product

$$OLG = G * H$$

by joining relation (3) and (5)

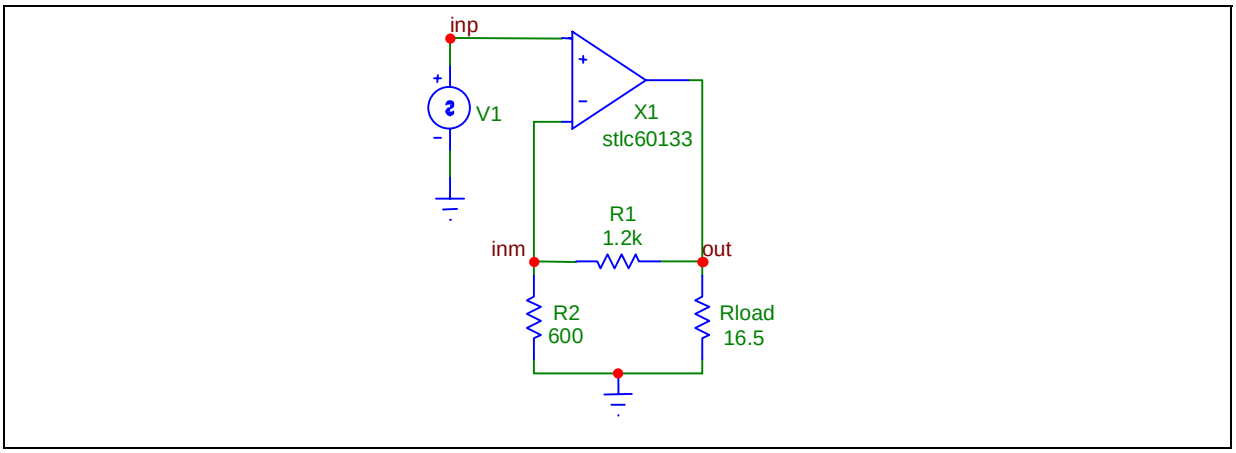
$$OLG = inm / (inp - inm)$$

that is still relation (1)

Test circuit schematic used for the evaluation of the OLG is shown in Figure 2.

As specified in [2], for proper device operating it is necessary to work with a gain level greater than 6, i.e. 15.6 dB.

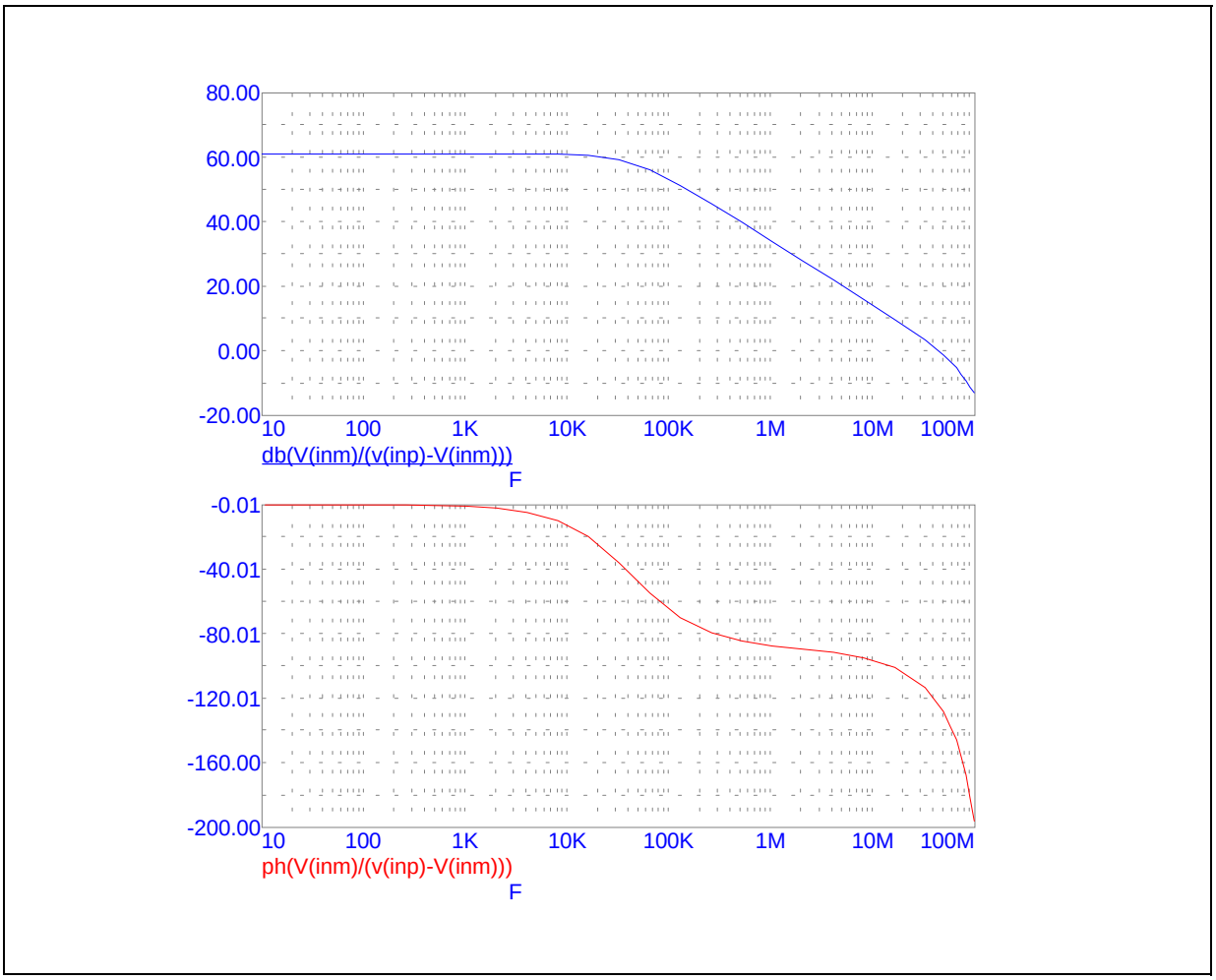
Figure 2. Open Loop Gain Test Circuit



PERFORMANCES

STLC60133 Model Open Loop differential Gain measured as specified in the previous paragraph is shown in Figure 3.

Figure 3. STLC60133 model Frequency Response



Comparison between model and design guaranteed performances, as obtained from simulation with the complete Eldo® description of the circuit, is shown in Table 1.

Table 1. Performances Comparison

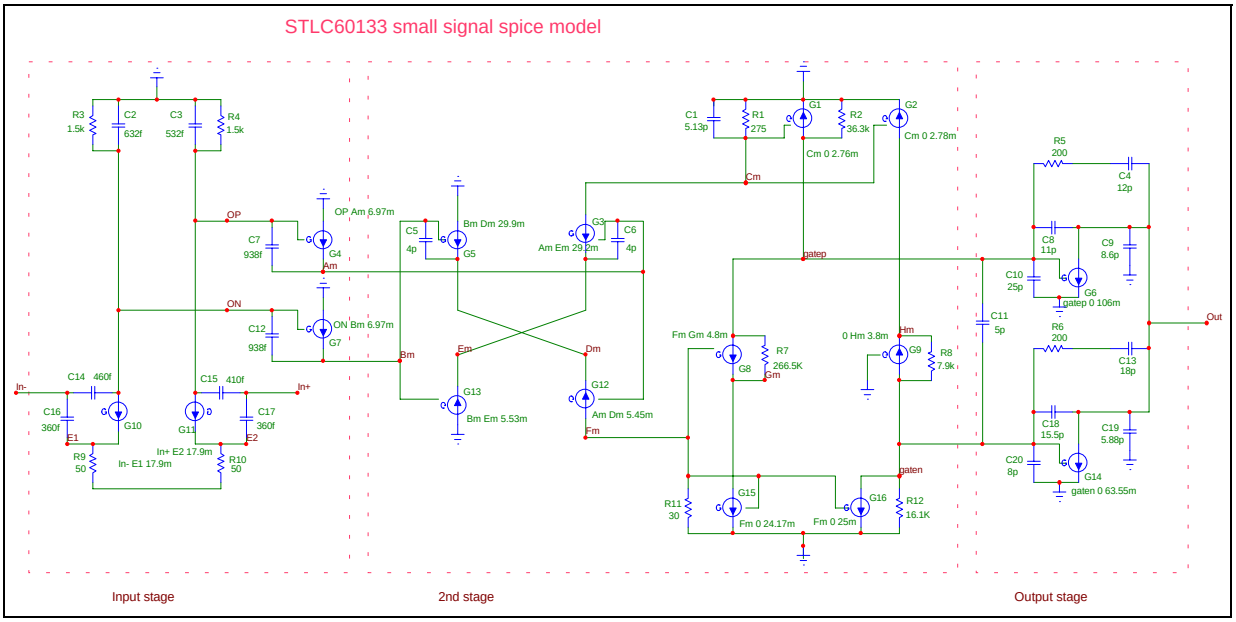
	Complete Model	STLC60133 Small Signal SPICE Model
DC gain [dB]	61.5	60.9
first pole [KHz]*	42.7	42.1
GBWP [MHz]	46.7	44.8
phase margin	65	56.3

* defined as -3dB frequency

SCHEMATIC AND SUBCIRCUIT LISTING

Model schematic is shown in figure 4.

Figure 4. STLC60133 Small Signal SPICE Model Schematic



SPICE Model Subcircuit listing can be copied in a file to be used as a subcircuit description for an electronic circuit analysis program such as Microcap ®

```
*  STLC60133 Small Signal Spice Subcircuit              DATE SEPT 2002
* Rev A
*
* Pin description
*                          non-inverting input
*                          |  inverting input
*                          |  |  output
*                          |  |  |
*                          |  |  |
*                          |  |  |
*                          |  |  |
*                          |  |  |
.SUBCKT STLC60133  1  2  3

*

* Input Stage

C2 ON 0 632F
C3 OP 0 532F
C7 Am OP 938F
C12 Bm ON 938F
C14 2 ON 460F
C15 1 OP 410F
C16 E1 2 360F
C17 E2 1 360F

R3 0 ON 1.5K
R4 0 OP 1.5K
R9 E1 20 50
R10 E2 20 50

G4 0 Am OP AM 6.97M
G7 0 Bm ON BM 6.97M
G10 ON E1 2 E1 17.9M
G11 OP E2 1 E2 17.9M


* 2nd Stage

C1 Cm 0 5.13P
C5 Dm Bm 4P
C6 Em Am 4P
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```
R1 0 Cm 275
R2 0 gatep 36.3K
R7 gatep Gm 266.5K
R8 Hm gaten 7.9K
R11 Fm 0 30
R12 gaten 0 16.1K

G1 gatep 0 CM 0 2.76M
G2 Hm 0 CM 0 2.78M
G3 Cm Em AM EM 29.2M
G5 0 Dm BM DM 29.9M
G8 gatep Gm FM GM 4.8M
G9 gaten Hm 0 HM 3.8M
G12 Fm Dm AM DM 5.45M
G13 0 Em BM EM 5.53M
G15 Gm 0 FM 0 24.17M
G16 gaten 0 FM 0 25M


* Output Stage

C4 3 6 12P
C8 3 gatep 11P
C9 0 3 8.6P
C10 0 gatep 25P
C11 gaten gatep 5P
C13 3 14 18P
C18 3 gaten 15.5P
C19 0 3 5.88P
C20 0 gaten 8P

R5 gatep 6 200
R6 gaten 14 200

G6 3 0 gatep 0 106M
G14 3 0 gaten 0 63.55M

*
.ENDS STLC60133
```

FURTHER ENHANCEMENT

Two digital pins (PWDN0 and PWDN1) allow the driver to work in full performance mode, in low-power mode or two intermediate bias states.

For the time being only full performance mode is modeled, but in the future a parametric model will simulate the effect of bias current on AC performances too.

BIBLIOGRAPHY

[1] Hageman, Steven C., "Spice techniques facilitate analysis of feedback circuits" EDN, September 29, 1988.

[2] STLC60133 XDSL LINE DRIVER datasheet.